



eZ80F91 Contest Kit

User Manual

PRELIMINARY

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**eZ80F91 Contest Kit
User Manual**



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Safeguards

The following precautions must be observed when working with the devices described in this document.



Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

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Introduction

The eZ80F91 Contest Kit is designed to support the eZ80F91 design contest sponsored by ZiLOG, Inc. It provides a general-purpose platform for creating a design based on ZiLOG's eZ80F91 microcontroller. The eZ80F91 MCU is a member of ZiLOG's eZ80Acclaim![™] product family, which offers on-chip Flash capability. The eZ80F91 Contest Kit features an eZ80F91 Module for which you must design a motherboard. See the [eZ80F91 Contest Kit Simple Motherboard Schematic](#) on page 31.

Kit Features

The key features of the eZ80F91 Contest Kit are:

- eZ80F91 Module:
 - eZ80F91 device operating at 50MHz, with 256KB of internal Flash memory and 8KB of internal SRAM memory
 - 512KB of off-chip SRAM memory
 - 1MB of off-chip Flash memory (footprint)
 - On-chip Ethernet Media Access Controller (EMAC)
 - Ethernet port
 - IrDA port
 - Real-Time Clock with battery backup
 - Two headers for attachment to connectors on the motherboard you design.
- Serial Smart Cable
- eZ80Acclaim![™] Software and Documentation CD-ROM
- CMX Systems TCP/IP stack CD-ROM
- Schematics for the eZ80F91 module and a simple motherboard



eZ80F91 Contest Kit Overview

The purpose of the eZ80F91 Contest Kit is to provide the contestant with a set of tools for designing an application based on the eZ80F91 microcontroller. You must construct an application motherboard that contains at least four connectors:

- A power connector for an external power supply.
- A ZDI connector to connect the finished application to a host PC running ZiLOG Developer Studio II Integrated Development Environment software (ZDS II).
- Two 50-pin receptacles into which you will plug the eZ80F91 Module.

A block diagram of the a typical motherboard design and a connected eZ80F91 Module is shown in Figure 1.

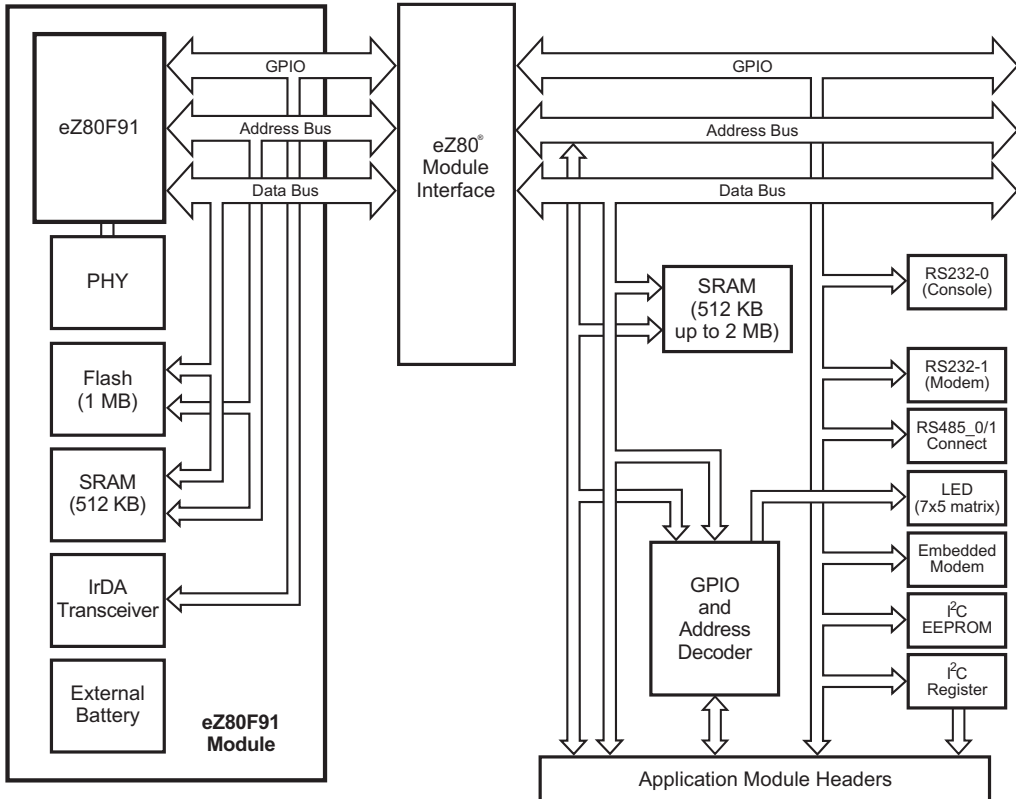
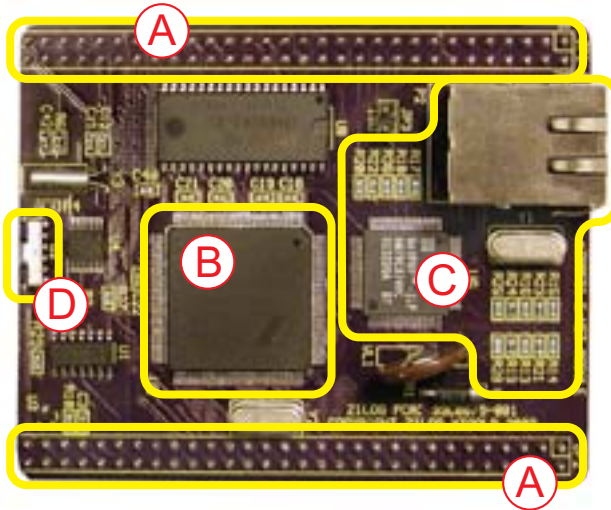


Figure 1. Typical Application Motherboard Block Diagram with eZ80F91 Module

Figure 2 is a photographic representation of the eZ80F91 Module segmented into its key blocks, as shown in the legend for the figure.



Note: Key to blocks A–C.

- A. eZ80F91 Module interfaces.
- B. eZ80F91 CPU.
- C. 10/100BaseT Ethernet Interface
- D. IrDA transceiver.

Figure 2. The eZ80F91 Module

The structures of the eZ80F91 Module and a simple motherboard are illustrated in the [Schematics](#) starting on page 31.



Application Motherboard Design

This section describes the requirements for designing an eZ80F91 module-compatible application motherboard.

eZ80F91 Module Interface

The eZ80F91 Module interface on your motherboard design consists of two 50-pin receptacles; a third receptacle can also be included to enable on-chip Flash memory programming. Each is described in the pages that follow.

Almost all of these receptacles' signals are connected directly to the CPU. Five input signals, in particular, offer options to the application developer by disabling certain functions of the eZ80F91 Module.

These five input signals¹ are:

- Enable Flash ($\overline{\text{EN_Flash}}$)
- Flash Write Enable ($\overline{\text{FlashWE}}$)
- Disable IrDA ($\overline{\text{DIS_IrDA}}$)
- $\overline{\text{F91_WE}}$
- RTC_V_{DD}

A description of these five signals follows.

Enable Flash. When active Low, the $\overline{\text{EN_Flash}}$ input signal enables the Flash chip on the eZ80F91 Module.

1. These input signals are only used if external Flash memory is present on the eZ80F91 Module. As shipped from the factory, external Flash is not installed.



Flash Write Enable. When active Low, the $\overline{\text{FlashWE}}$ input signal enables write operations on the Flash boot block of the eZ80F91 Module.

Disable IrDA. When the $\overline{\text{DIS_IrDA}}$ input signal is pulled Low, the IrDA transceiver, located on the eZ80F91 Module, is disabled. As a result, UART0 can be used with the RS232 or the RS485 interfaces on the eZ80[®] Development Platform.

F91_WE. When the $\overline{\text{F91_WE}}$ signal is active Low, internal Flash on the eZ80F91 Module is enabled for writing. This signal is inverted from the $\overline{\text{WP}}$ signal of on the eZ80F91 Module.

RTC_V_{DD}. RTC_V_{DD} is a test point for the Real Time Clock power supply.

Peripheral Bus Connector

Figure 3 illustrates the pin layout of the Peripheral Bus Connector in the 50-pin header on a typical application motherboard. Table 1 identifies the pins and their functions.

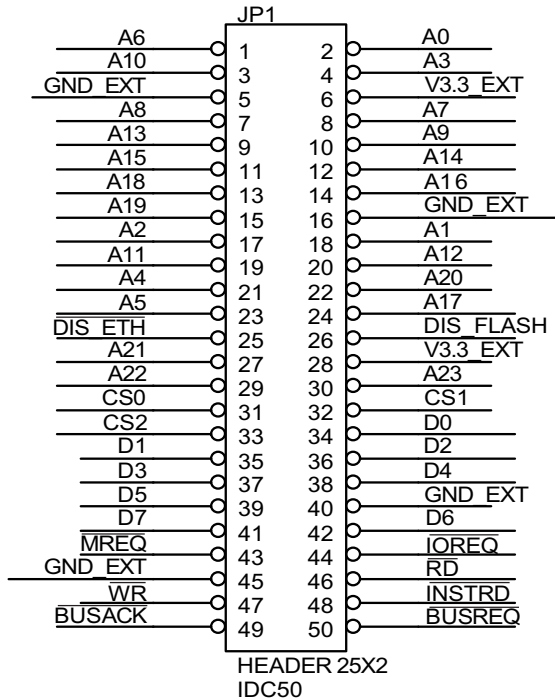


Figure 3. Typical Application Motherboard Peripheral Bus Connector Pin Configuration



Table 1. Typical Application Motherboard Peripheral Bus Connector Identification—JP1^{1,3}

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal ²
1	A6	Bidirectional		Yes
2	A0	Bidirectional		Yes
3	A10	Bidirectional		Yes
4	A3	Bidirectional		Yes
5	GND			
6	V _{DD}			
7	A8	Bidirectional		Yes
8	A7	Bidirectional		Yes
9	A13	Bidirectional		Yes
10	A9	Bidirectional		Yes
11	A15	Bidirectional		Yes
12	A14	Bidirectional		Yes
13	A18	Bidirectional		Yes
14	A16	Bidirectional		Yes
15	A19	Bidirectional		Yes

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics [on pages 32 through 34](#).
2. The Power and Ground nets are connected directly to the eZ80F91 device.
3. Additional note: external capacitive loads on RD, WR, IORQ, MREQ, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91’s Peripheral Power-Down Register.



Table 1. Typical Application Motherboard Peripheral Bus Connector Identification—JP1^{1,3} (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal ²
16	GND			
17	A2	Bidirectional		Yes
18	A1	Bidirectional		Yes
19	A11	Bidirectional		Yes
20	A12	Bidirectional		Yes
21	A4	Bidirectional		Yes
22	A20	Bidirectional		Yes
23	A5	Bidirectional		Yes
24	A17	Bidirectional		Yes
25	DIS_ETH	Output	Low	No
26	EN_Flash	Output	Low	No
27	A21	Bidirectional		Yes
28	V _{DD}			
29	A22	Bidirectional		Yes
30	A23	Bidirectional		Yes

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics [on pages 32 through 34](#).
2. The Power and Ground nets are connected directly to the eZ80F91 device.
3. Additional note: external capacitive loads on RD, WR, IORQ, MREQ, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.



**Table 1. Typical Application Motherboard
Peripheral Bus Connector Identification—JP1^{1,3} (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal ²
31	CS0	Input	Low	Yes
32	CS1	Input	Low	Yes
33	CS2	Input	Low	Yes
34	D0	Bidirectional		Yes
35	D1	Bidirectional		Yes
36	D2	Bidirectional		No
37	D3	Bidirectional		Yes
38	D4	Bidirectional		Yes
39	D5	Bidirectional		Yes
40	GND			
41	D7	Bidirectional		Yes
42	D6	Bidirectional		Yes
43	MREQ	Bidirectional	Low	Yes
44	IORQ	Bidirectional	Low	Yes
45	GND			

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics [on pages 32 through 34](#).
2. The Power and Ground nets are connected directly to the eZ80F91 device.
3. Additional note: external capacitive loads on RD, WR, IORQ, MREQ, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.



Table 1. Typical Application Motherboard Peripheral Bus Connector Identification—JP1^{1,3} (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal ²
46	RD	Bidirectional	Low	Yes
47	WR	Bidirectional	Low	Yes
48	INSTRD	Input	Low	Yes
49	BUSACK	Input	Pull-Up 10K Ω ; Low	Yes
50	BUSREQ	Output	Pull-Up 10K Ω ; Low	Yes

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics [on pages 32 through 34](#).
2. The Power and Ground nets are connected directly to the eZ80F91 device.
3. Additional note: external capacitive loads on RD, WR, IORQ, MREQ, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

I/O Connector

Figure 4 illustrates the pin layout of the I/O Connector in the 50-pin header on the application motherboard. Table 2 identifies the pins and their functions.

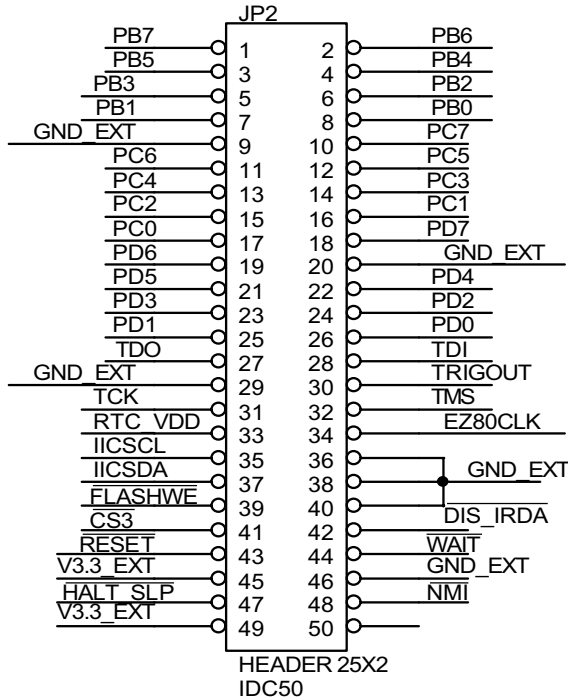


Figure 4. Typical Application Motherboard I/O Connector Pin Configuration



**Table 2. Typical Application Motherboard
I/O Connector Identification—JP2¹**

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal ²
1	PB7	Bidirectional		Yes
2	PB6	Bidirectional		Yes
3	PB5	Bidirectional		Yes
4	PB4	Bidirectional		Yes
5	PB3	Bidirectional		Yes
6	PB2	Bidirectional		Yes
7	PB1	Bidirectional		Yes
8	PB0	Bidirectional		Yes
9	GND			
10	PC7	Bidirectional		Yes
11	PC6	Bidirectional		Yes
12	PC5	Bidirectional		Yes
13	PC4	Bidirectional		Yes
14	PC3	Bidirectional		Yes
15	PC2	Bidirectional		Yes
16	PC1	Bidirectional		Yes
17	PC0	Bidirectional		Yes
18	PD7	Bidirectional		Yes

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics [on pages 32 through 34](#).
2. The Power and Ground nets are connected directly to the eZ80F91 device.



**Table 2. Typical Application Motherboard
I/O Connector Identification—JP2¹ (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal ²
19	PD6	Bidirectional		
20	GND			
21	PD5	Bidirectional		Yes
22	PD4	Bidirectional		Yes
23	PD3	Bidirectional		Yes
24	PD2	Bidirectional		Yes
25	PD1	Bidirectional		Yes
26	PD0	Bidirectional		Yes
27	TDO	Input		Yes
28	TDI/ZDA	Output		Yes
29	GND			
30	TRIGOUT	Input	High	
31	TCK/ZCL	Output		Yes
32	TMS	Output	High	Yes
33	RTC_V _{DD}			
34	EZ80CLK	Input		Yes
35	SCL	Bidirectional		Yes
36	GND			

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics [on pages 32 through 34](#).
2. The Power and Ground nets are connected directly to the eZ80F91 device.



**Table 2. Typical Application Motherboard
I/O Connector Identification—JP2¹ (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal ²
37	SDA	Bidirectional		Yes
38	GND			
39	FlashWE	Output	Low	No
40	GND			
41	CS3	Input	Low	Yes
42	DIS_IrDA	Output	Low	No
43	RESET	Bidirectional	Low	Yes
44	WAIT	Output	Pull-Up 10K Ω ; Low	Yes
45	V _{DD}			
46	GND			
47	HALT_SLP	Input	Low	Yes
48	NMI	Output	Low	Yes
49	V _{DD}			
50	Reserved			

Notes:

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics [on pages 32 through 34](#).
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Internal On-Chip Flash Memory

To program internal on-chip Flash memory, the JP3 shunt on the eZ80F91 Module must be installed. Table 3 lists the setting for the JP3 jumper that is resident on the eZ80F91 Module.



Table 3. Jumper, eZ80F91 Module

Symbol	Jumper Name	Shunt Status	Function	Affected Device
JP3	Write Enable (WR_EN)	In	On-chip Flash is enabled for writing.	On-chip Flash
		Out	On-chip Flash memory is write-protected.	On-chip Flash



eZ80F91 Module

This section describes the eZ80F91 Module hardware, its interfaces and key components, including the CPU, real-time clock, IrDA transceiver, and memory.

Functional Description

The eZ80F91 Module is a compact, high-performance module specially designed for the rapid development and deployment of embedded systems. Additional devices such as serial ports, LED matrices, GPIO ports, and I²C devices can be supported by your application motherboard.

Despite its small footprint, the eZ80F91 Module provides a CPU, Flash memory, Ethernet interface, SRAM, an IrDA transceiver, and a real-time clock with a back-up battery. This module is powered by the eZ80F91 microcontroller, a new member of ZILOG's eZ80Acclaim!TM product family. The eZ80F91 Module can also be used as a stand-alone development tool when provided with an external power source.

Fast Buffer

A Fast Buffer is located on the data bus to Flash memory. The purpose of this Fast Buffer is to avoid bus contention that can exist due to the slow turn-off time of Flash memory and the fast bus turn-around time of the eZ80F91 device (a generic feature of the eZ80Acclaim!TM family when is used in native mode). The discussion that follows references Figure 5.

Bus contention can occur when two or more devices drive a common bus. CS0 on the eZ80F91 device drives the Flash CE. Upon accessing Flash memory, CS0 is driven High a maximum of 8.8ns after the next rising edge of the CPU Clock (T₆—please refer to the External Memory Read Timing diagram in the eZ80F91 Product Specification (PS0192) for assis-tance). The Flash turn-off time (T_{OD}) is 25ns—the duration from OE or



CE going High to Flash output drivers in a high-impedance state. For further information, see the MT28F008 data sheet on www.micron.com.

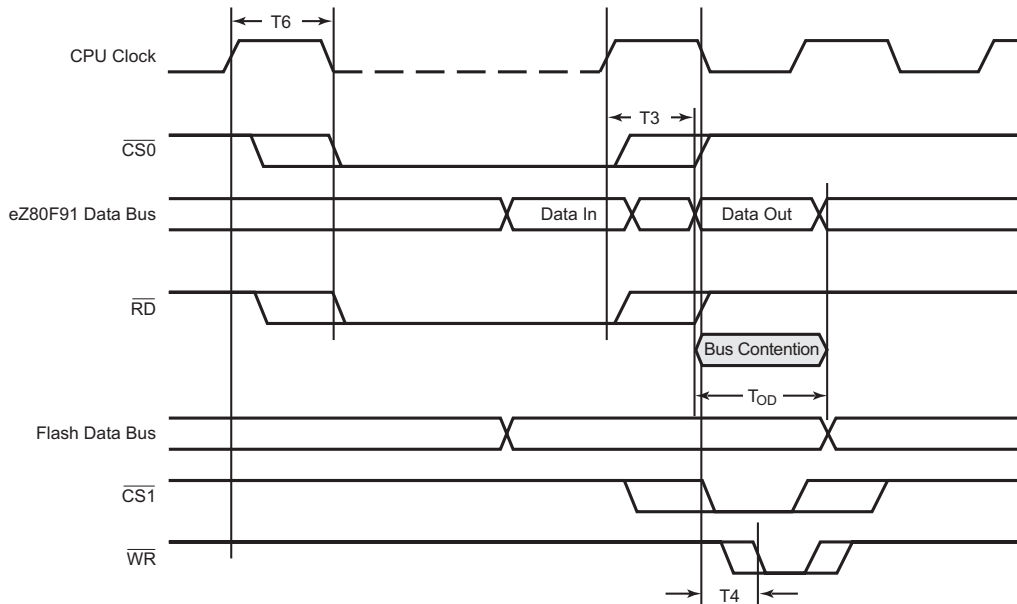


Figure 5. Possible Bus Contention without Fast Buffer

Essentially, after the eZ80F91 device accesses Flash memory, a time duration of $8.8\text{ns} + 25\text{ns} = 33.8\text{ns}$ can transpire before Flash memory stops driving the data bus. At that time, the eZ80F91 device is well into the next bus cycle. Assuming this next cycle is the Memory Write cycle, then the data output of the eZ80F91 device is valid not later than $T3 = 7.5\text{ns}$, and the write pulse is asserted not later than 4.5ns after the falling edge of the CPU Clock (14.5ns from the rising edge if the CPU Clock is 50MHz). The duration of bus contention, T_{CON} , is $33.8\text{ns} - 7.5\text{ns} = 26.3\text{ns}$. Refer to the External Memory Write Timing diagram in the eZ80F91 Product Specification (PS0192) for assistance.



With the addition of a Fast buffer, Flash turn-off time is reduced from 25 ns to 5.5 ns. Bus contention can still occur, but the amount of time it consumes is not $T_{\text{CON}} = 26.3 \text{ ns}$ but rather $T_{\text{CON}} = (8.8 \text{ ns} - 7.5 \text{ ns} + 5.5 \text{ ns}) = 6.8 \text{ ns}$. At this faster rate, data that is being written does not become corrupted because the write pulse is not yet asserted.

As of the date of publication of this document, ZiLOG has not completed an analysis of the effect that this 6.8 ns period of bus contention has on the design. An Application Note from [Cypress Semiconductor](#) titled *NoBL SRAM and Bus Contention* further explains this bus contention issue.

Physical Dimensions

The footprint of the eZ80F91 Module PCB is 63.5 mm x 78.7 mm. With an RJ-45 Ethernet connector, the overall height is 25 mm. See Figure 6.

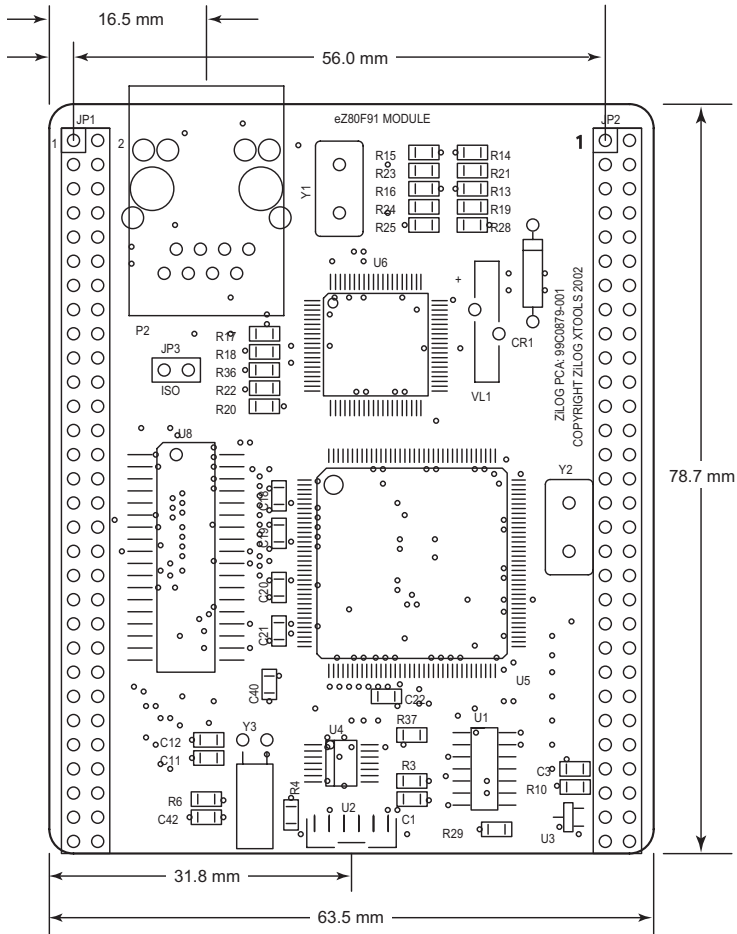


Figure 6. Physical Dimensions of the eZ80F91 Module

Figure 7 illustrates the top layer silkscreen of the eZ80F91 Module.

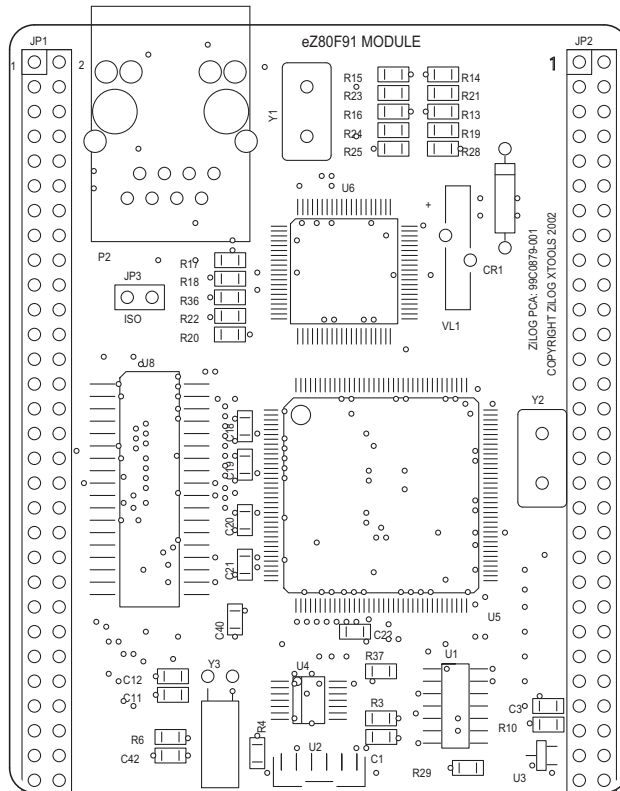


Figure 7. eZ80F91 Module—Top Layer

Figure 8 illustrates the bottom layer silkscreen of the eZ80F91 Module.

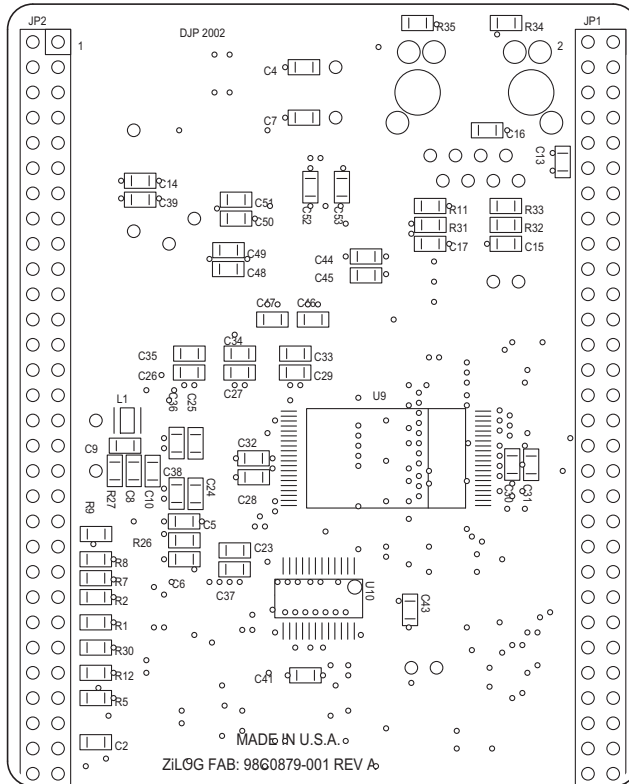


Figure 8. eZ80F91 Module—Bottom Layer

Operational Description

The purpose of the eZ80F91 Module as a feature of the eZ80F91 Contest Kit is to provide application developers with a design platform that enables them to make use of such eZ80F91 device features of the as on-chip EMAC, SRAM, Flash, etc.



eZ80F91 Module Memory

Static RAM

The eZ80F91 Module features 512 KB of fast SRAM. Access speed is typically 12ns, allowing zero-wait-state operation at 50MHz. With the CPU at 50MHz, SRAM can be accessed with zero wait states in eZ80 mode. CS1_CTL (CS1) can be set to 08h (no wait states).

Flash Memory

The eZ80F91 Module features 256KB of on-chip Flash memory, which can be programmed a single byte at a time, or in bursts of up to 128 bytes. Write operations can be performed using either memory or I/O instructions. Erasing bytes in Flash memory returns them to a value of FFh. Both the MASS ERASE and PAGE ERASE operations are self-timed by the Flash controller, leaving the CPU free to execute other operations in parallel. Upon power-up, the on-chip Flash memory is located in the address range 000000h–03FFFFh. Four wait states are programmed in Flash control register F8h.

On-chip Flash memory is prioritized over all external Chip Selects, can be enabled or disabled (power-on enabled), and can be programmed within any 256KB address space in the 16MB address range.

The eZ80F91 Module features the following memory configurations:

- On-chip SRAM: 8KB
- Off-chip SRAM: 512KB
- On-chip Flash: 256KB

Reset Generator

An onboard supervisory chip is connected to the eZ80F91 Reset input pin. It performs reliable Power-On Reset functions, generating a reset pulse with a duration of 200ms if the power supply drops below 2.93V. This reset pulse ensures that the board always starts in a defined condi-



tion. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80F91 Contest Kit with a low-impedance output (e.g. a 100-Ohm push button).

IrDA Transceiver

An onboard IrDA transceiver (ZiLOG ZHX1810) is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, IR_SD). The IrDA transceiver is of the LED type 870nm Class 1.

The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80F91 device.

To use the UART0 as a console or to save power, the transceiver can be disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IR_SD) High or by pulling the DIS_IRDA pin on the I/O connector Low. The shutdown feature is used for power savings. To enable the IrDA transceiver, DIS_IRDA is left floating and PD2 is pulled Low.

The RxD and TxD signals on the transceiver perform the same functions as a standard RS232 port. However, these signals are processed as IrDA 3/16 coding pulses (sometimes called IrDA encoder/decoder pulses). When the IrDA function is enabled, the final output to the RxD and TxD pins are routed through the 3/16 pulse generator.

Another signal that is used in the eZ80F91 Module's IrDA system is Shut_Down (SD). The SD pin is connected to PD2 on the eZ80F91 Module. The IrDA control software on the user's wireless device must enable this pin to wake the IrDA transceiver. The SD pin must be set Low to enable the IrDA transceiver. On the eZ80F91 Module, a two-input OR gate is used to allow an external pin to shut down the IrDA transceiver. Both pins must be set Low to enable this function.

Figure 9 highlights the eZ80F91 Module IrDA hardware connections.

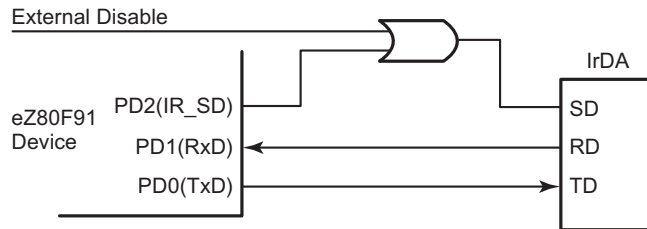


Figure 9. IrDA Hardware Connections

The eZ80F91 Module features an Infrared Encoder/Decoder register that configures the IrDA function. This register is located at address 0BFh in the internal I/O register map.

The Infrared Encoder/Decoder register contains three control bits. Bit 0 enables or disables the IrDA encoder/decoder block. Bit 1, if it is set, enables received data to pass into the UART0 Receive FIFO data buffer. Bit 2 is a test function that provides a loopback sequence from the TxD pin to the RxD input.

Bit 1, the Receive Enable bit, is used to block data from filling up the Receive FIFO when the eZ80F91 Module is transmitting data. Because IrDA signal passes through the air as its transmission medium, transmitted data can also be received. This Receive Enable bit prevents this data from being received. After the eZ80F91 Module completes transmitting, this bit is changed to allow for incoming messages.

The code that follows provides an example of how this function is enabled on the eZ80F91 Module.

```
//Init_IRDA
// Make sure to first set PD2 as a port bit, an output
// and set it Low.

PD_ALT1 &= 0xFC; // PD0 = uart0tx, PD1 = uart0_rx
PD_ALT2 |= 0x03; // Enable alternate function
```



```
UART_LCTL0= 0x80; // Select dlab to access baud rate
                // generator
BRG_DLRL0=0x2F;  // Baud rate Masterclock ÷
                // (16*baudrate)
BRG_DLRH0=0x00; // High byte of baud rate
UART_LCTL0=0x00; // Disable dlab
UART_FCTL0=0xC7; // Clear tx FIFO, enable FIFO
UART_LCTL0=0x03; // 8bit, N, 1 stop
IR_CTL = 0x03;   // enable IRDA Encode/decode and
                // Receive
                // enable bit.
                // IRDA_Xmit

IR_CTL = 0x01;   // Disable receive
Putchar(0xb0);  // Output a byte to the uart0 port.
```

Flash Loader Utility

The Flash Loader utility integrated within ZDS II allows the user a convenient way to program on-chip Flash memory. Please refer to the ZiLOG Developer Studio—eZ80Acclaim!TM User Manual (UM0144) for more details.



ZDSII

ZiLOG Developer Studio II (ZDSII) Integrated Development Environment is a complete stand-alone system that provides a state-of-the-art development environment. Based on the Windows® Win98SE/NT4.0-SP6/Win2000-SP2/WinXP user interfaces, ZDSII integrates a language-sensitive editor, project manager, C-Compiler, assembler, linker, librarian, and source-level symbolic debugger that supports the eZ80F91 device.

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Troubleshooting

Overview

Before contacting ZiLOG Customer Support to submit a problem report, please follow these simple steps. If a hardware failure is suspected, contact a local ZiLOG representative for assistance.

IrDA Port Not Working

If you plan on using the IrDA transceiver on the eZ80F91 Module, make sure the hardware is set up as follows:

- Jumper J2 must be OFF (to enable the control gate that drives the IrDA device)
- Set port pin PD2 Low. When this port pin and Jumper J2 are turned OFF, the IrDA device is enabled.
- Install a jumper on connector J6 across pin names *con_dis* and *GND* to disable the console serial port driver

Contacting ZiLOG Customer Support

For additional troubleshooting solutions, see ZDS II Online Help.

For valuable information about hardware and software development tools, visit [ZiLOG Customer Support](#) online. Download the latest released version of [ZiLOG Developer Studio!](#)

Get the latest [software updates](#) from ZiLOG as soon as they are available!

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eZ80F91 Module

Figures 11 through 13 diagram the layout of the eZ80F91 Module. Ethernet circuiting devices are not loaded on the eZ80F91 Module. However, these devices appear in the following schematics for reference purposes.

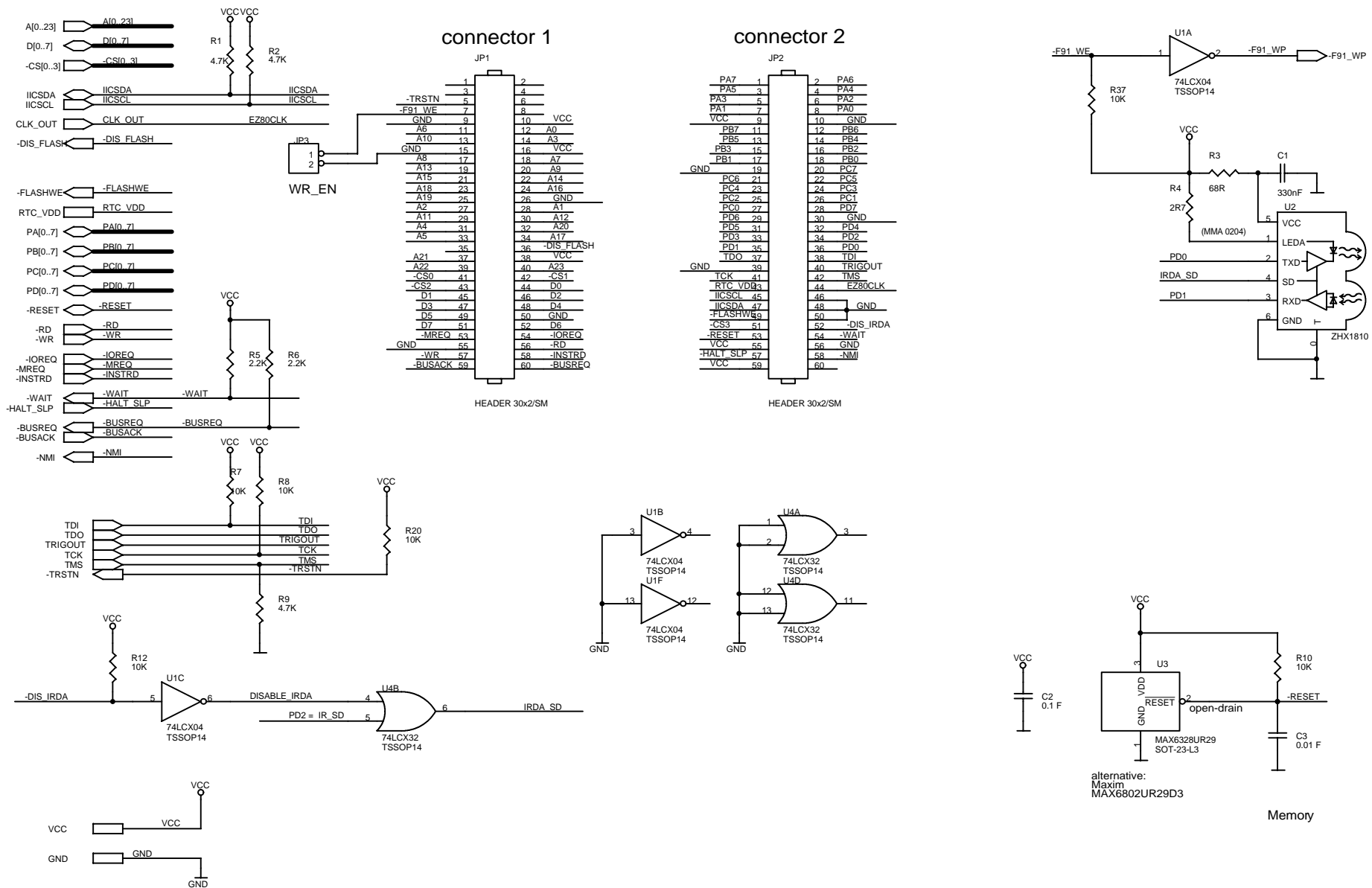


Figure 11. eZ80F91 Module Schematic Diagram, #1 of 3,,Connectors and Miscellaneous

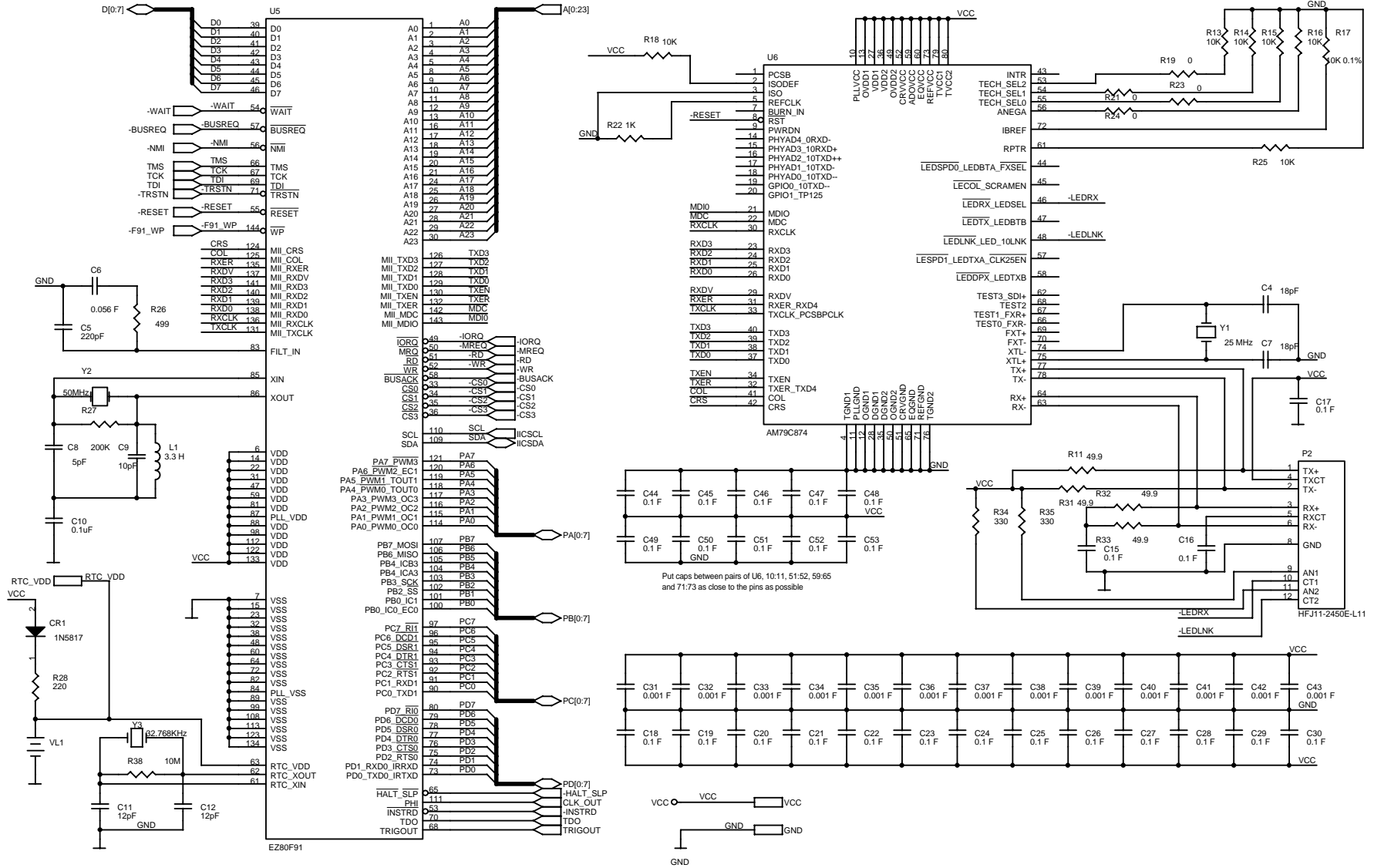


Figure 12. eZ80F91 Module Schematic Diagram, #2 of 3,,CPU and PHY



Customer Feedback Form

If you note any inaccuracies while reading this User Manual, please copy and complete this form, then mail or fax it to ZiLOG (see Return Information, below). We also welcome your suggestions!

eZ80F91 Contest Kit

Serial # or Board Fab #/Rev. #

Software Version

Document Number

Host Computer Description/Type

Customer Information

Name

Country

Company

Phone

Address

Fax

City/State/Zip

E-Mail

Return Information

ZiLOG

System Test/Customer Support

532 Race Street

San Jose, CA 95126

Phone: (408) 558-8500

Fax: (408) 558-8536

[ZiLOG Customer Support](#)

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.
